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Vicinal Si(hhm) surfaces: templates for nanostructures fabrication

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Abstract- Fabrication of well ordered low dimensional structures on clean and metal-decorated stepped Si(hhm) surfaces is discussed. The atomic structure of clean Si(557)7×7 and Si(556)7×7 surfaces fabricated using special annealing procedures and metal-decorated Ag/Si(557) and Gd/Si(557) systems has been studied using high resolution scanning tunneling microscopy and low energy electron diffraction. The investigations demonstrate feasibility of fabrication of 1D- and 2D-structures of gadolinium and silver atoms on the Si(557) surface.

Keywords- Density functional theory (DFT); Full Potential Linearized Augmented Plane Waves (FPLAPW); Spin polarized calculations; Density of States (DOS); Band Structures;Generalized Gradient Approximation (GGA).

1. INTRODUCTION

Nanostructured materials and low-dimensional systems (quantum dots, wires and nanostripes) are both from fundamental and practical importance due to unique physical properties and potential applications in nanoelectronics. Natural defects of stepped Si(hhm) surfaces obtained by miscut off the low-index silicon (111) plane can be utilized for fabrication of regular arrays of nanoobjects (atomic chains and stripes on terraces and/or steps) with controlled dimensions and periodicities [1][14]. However, despite the high interest to these perspective semiconducting templates, preparation of well-ordered regular stepped silicon substrates with desirable atomic structure and step periodicity is rather complicated procedure.

Usually, preparation of atomically clean on-plane and vicinal Si(111)7×7 surfaces [15] in ultra high vacuum (UHV) includes flash heating at 1200-1300°C (to remove contaminations and protective oxide layer) and controllable cool down to temperatures below 870ºC (temperature of the (1×1)→(7×7) phase transition). Si(111) surfaces prepared by the above mentioned method, as a rule, demonstrate (7×7) reconstruction stable in UHV at room temperature. Si(111) wafers are usually heated by electric current that allows to achieve high temperatures on the silicon wafer without substantial increase of the pressure in the preparation chamber. In the case of direct current heating, the temperature on the sample can be changed rather fast and minor increase of the pressure in the UHV chamber is usually not critical for preparation of clean silicon surfaces without adsorbate contamination. However, during the direct current heating one should keep in mind electromigration of silicon atoms across the surface [16][17]. The electromigration phenomena at certain current directions and temperatures lead to increase of the terrace widths and step bunching on vicinal silicon surfaces. In these cases, the atomic structure of surfaces with the same miscut prepared using different annealing strategies can be different [16][19]. Figure 1 summarizes the published data about the influence of the electric field on the atomic structure of the Si(111) surfaces with small (not exceeding several degrees) miscuts off the low-index plane [18]. As Fig. 1 illustrates, above the (1×1)→(7×7) phase transition temperature there are several temperature ranges where change of the current direction («step-up» and «step-down») leads to substantial change of the steps' regularity and heights. In the temperature range I between 830º and 1000ºC with electric current in step-up direction, regular monatomic step arrays (R) can be fabricated while at the step-down current direction, step bunching (SB) leading to a formation of irregular mono- and multiatomic step systems can be observed (Fig. 1). In the temperature range II (1000-1180ºC) the reversed effect is observed: Regular monatomic step arrays can be fabricated using a step-down current direction while heating with a step-up current direction lead to the step bunching. The influence of the electric field on the regularity of the step arrays and the step heights is related to the temperature dependence of the silicon adatom's electromigration which is still not known in detail. It is generally believed that heating of vicinal Si(111) surfaces using electric current directed parallel to steps allows to minimize the electromigration processes at high temperatures. Nevertheless, even in this case, SB cannot be avoided completely, and the atomic structure of the

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fabricated vicinal silicon surfaces can depend on the temperature regimes of the sample heating.

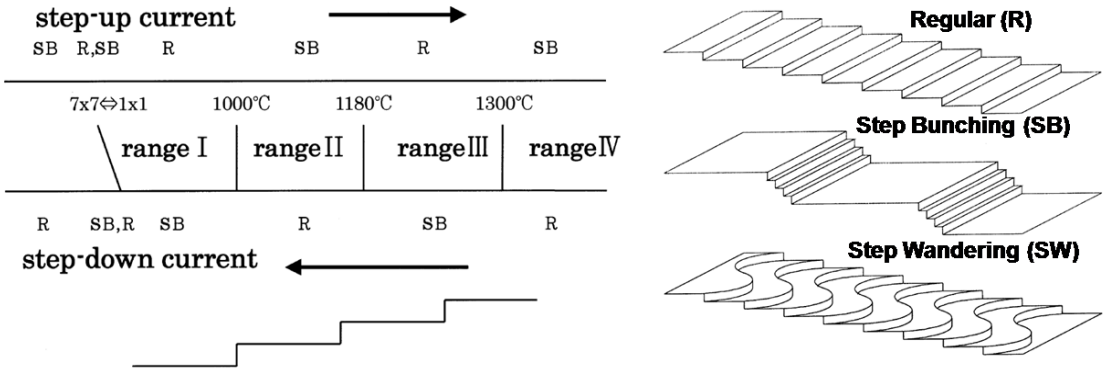

Fig. 1. Influence of the temperature and the current direction on the step periodicity on vicinal Si(111) [18].

Although there is a large amount of experimental data about the electromigration processes and step bunching on the vicinal Si(111) surfaces with small miscuts, the influence of the annealing procedure on the step regularity for high-index Si(hhm) surfaces with large miscut angles is not well established. This is also related to the fact that surface atomic structure and the step periodicity at large miscuts can be modified by step-step interaction which becomes stronger at decreasing distance between neighbouring steps [20].

The aim of the present study is related to optimization of the regular step array fabrication procedure on clean vicinal Si(557)7×7 and Si(556)7×7 surfaces, preparation of metal nanostructures on these substrates, and investigation of the atomic structure of clean and metal decorated Si(hhm) surfaces by scanning tunneling microscopy (STM) and low energy electron diffraction (LEED) techniques. It was found that special regime of preparation allows one to minimize step bunching effects and fabricate regular systems of terraces and steps on Si(hhm)7×7 surfaces with minimal deviation from the original miscut. High resolution STM data suggest that vicinal Si(hhm) surfaces can consist of regular on atomic scale sequences of terraces and triple steps with different configurations without valley periodicity breaking on near micron areas. Such regular triple step arrays can be used for fabrication of 1D and 2D nanostructures of metals (Ag, Gd) with unique physical properties on semiconducting surfaces.

2. EXPERIMENT

The experiments were carried out in the UHV chamber of a LAS-3000 spectrometer (RIBER) equipped with Auger electron spectroscopy (AES), LEED, and STM techniques. A base pressure in the analytical chamber was kept below 8×10−11 Torr. STM studies of the Si(hhm) surface atomic structure were performed at room temperature (RT) using a commercial STM GPI-300. STM tips were fabricated from single crystalline and polycrystalline tungsten ingots using electrochemical etching in 2M NaOH. Prior to mounting onto the scanning head, the etched tungsten tips were cleaned and sharpened in UHV using electron beam flash heating (800–1300°C) and co-axial Ar+ ion sputtering at an argon gas pressure p=5×10−5 Torr and ion energy E=600 eV [21].

Si(557) and Si(556) single crystalline polished samples (0.5×3×8 mm, n-type, P-doped, 2×1014 cm−3, 25 Ω·cm at RT) with 9.45° and 5.05° miscuts off the Si(111) in the (-1 -1 2) direction were utilized. After loading into the UHV chamber, the samples were degassed at 600°C for 15-20 hours. During the outgassing, the pressure in the system was kept in the low 10−10 Torr region. Regular step arrays on clean Si(hhm) surfaces were fabricated using special direct current heating procedures. They involved flash heating at high temperatures above the phase transition point and gradual cooling to temperatures below the (1×1)→(7×7) phase transition. The temperature of the silicon wafers was measured by an optical pyrometer.

Deposition of gadolinium and silver atoms was carried out from the well outgased tungsten basket in preparation chamber of the LAS-3000 spectrometer immediately after preparation of clean Si(hhm) surfaces. The substrate temperature during gadolinium and silver deposition was slightly above RT. The pressure during the metal deposition did not exceed 1×10-9 Torr. The metal overlayer thickness was controlled using a quartz thickness monitor. The deposition rate did not exceed 1 Å/min. The absence of contaminants on the surfaces was confirmed by AES and

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STM.

3. RESULTS AND DISCUSSION

Atomic structure of clean Si(hhm) surfaces

Fabrication of the regular triple step array with a periodicity of 5.73 nm on the Si(557) surface was demonstrated in [2]. The number of periodicity breakings in some Si(557) surface regions was as low as 1 per 40 triple step sequences [2]. The reported surface preparation procedure involved flash heating to 1230°C, cooling to 1060°C in 30 sec, quench to 830°C, postannealing at 830°C for 15 min, and cool down to RT. The current direction was parallel to the step edges for minimization of the mass-transport [2]. From STM data the periodicity of the step array was identified as 17 atomic rows in <110> direction while the triple step orientation was defined as (112). In several studies the precise atomic structure of the triple steps on Si(557) was investigated by LEED [3] and STM [4]. According to the LEED studies [3] the triple steps on Si(557) can be approximated by the (113) rather than (112) plane. In Ref. [4] the regular triple step staircase with a periodicity of ~5.3 nm fabricated on the silicon substrate with original (557) orientation was studied with STM. It was supposed that fabricated regular triple step array corresponds to the Si(7 7 10) surface orientation with a 10.02º miscut in $\left[\bar{1}\bar{1}2\right]$ crystallographic direction. Using atomically resolved STM data the authors proposed the model of a nonuniform triple step consisting on consecutive single and (100)-oriented double steps, as Fig. 2 illustrates.

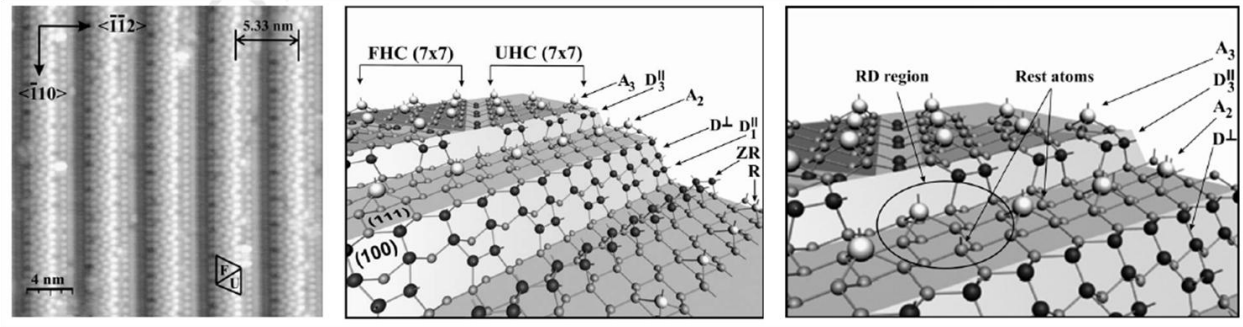

Fig. 2. STM image of Si(7 7 10) with 5.3 nm period (left) and triple step model (centre and right) proposed in Ref. [4]. The triple step consists on consecutive single step, small Si(111) terrace and double step having rows of $D_{\parallel}$ and $D_{\perp}$ dimers and additional row and zig-zag row at the bottom of the double step [4].

Previous studies [2][4] demonstrate that application of the same annealing procedure to the vicinal surfaces with the same initial miscut can lead to fabrication of different step arrays with periodicities of 5.7 nm [2] and 5.3 nm [4]. These inconsistencies in experimental data can be related to increase of the terrace widths after continuous annealing of the Si(557) surface near the phase transition temperature. It was demonstrated in Refs. [7][8] that regular step systems with minimal deflection of the local surface orientation from Si(557) can be obtained even at current perpendicular to the step edges. As an example, special annealing procedure with direct current perpendicular to steps allowed to fabricate a regular Si(223) triple step staircase [8].

Figures 3(a-c) and 3(d-f) show STM images of the regular triple step arrays fabricated on the Si(557) and Si(556) surfaces, respectively. Cross-sections of the images presented in Figs. 3(c) and 3(f) reveal the triple step periodicity close to 6 and 12 nanometers, respectively. Note that on the Si(557) sample we observed surface areas with lateral dimensions exceeding 0.5 mcm without periodicity breaking at the atomic scale. As an example, Fig. 3(a) shows a 250×250 nm2 surface area with atomically accurate triple step staircase. To avoid increase of the Si(111) terrace widths and SB on the Si(hhm) surfaces we utilized a special annealing strategy using direct current perpendicular to the step edges (step-up direction). After loading into UHV chamber the sample was degassed in 15-20 hours at temperatures below 650ºC. Then, after cooling to RT, the sample was flashed at 1250--1300ºC, cooled in 20-30 seconds to 900-950ºC (that corresponds to range I with regular steps for step-up current direction on Fig. 1), annealed at this temperature for 1 minute, cooled the sample to 600-650ºC in 15 minutes and annealed the sample at this

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temperature for a long time (from 20 to 60 minutes) to get ordered steps and terraces. STM studies of the Si(hhm) surfaces prepared with different durations and temperatures of the postannealing showed the importance of the right temperature regime at this last stage. The postannealing is necessary to order Si(111) terraces and achieve atomically accurate step array, however, the temperature should be well below the (1×1) → (7×7) phase transition temperature to avoid growth of the Si(111)7×7 terraces and SB. For Si(557) and Si(556) surfaces "safe" postannealing temperature range was found between 600 and 650°C. At these temperatures we could avoid the growth of the (111)-oriented terraces and appearance of the atomic scale irregularities in the step array at both current directions (parallel and perpendicular to steps). As a result, the local orientations of the surface regions containing regular triple step arrays was very close to the macroscopic orientation of the vicinal samples, as Fig. 3 illustrates.

Atomically resolved STM data showed that for the investigated Si(hhm) surfaces there are a several possible configurations of the triple steps. Two STM images of the triple steps from the regular Si(557) and Si(556) surfaces are presented on Fig. 3(c) and 3(f), respectively. For the both step systems, STM data demonstrate nonuniform structure of the triple steps consisting on monatomic step (indicated as S on Fig. 3), small Si(111) terrace, and double step (D) with orientation close to (113). STM studies revealed that mini-terrace between single and double steps can contain different number of adatom rows depending on the width of the large Si(111) terrace. The presence of different triple step configurations on the same triple step arrays indicates that step periodicity on the Si(hhm) surfaces depends not only on the exact atomic structure of the steps and terraces. The step periodicity can be influenced by appearance of the adsorbate and doping atoms at the step edges during high temperature sample treatments and step-step interaction substantial at large miscut angles [20].

STM images of the triple steps on Fig. 3 reveal parallel and perpendicular dimers on the double steps and defects on the Si(111) mini-terrace and steps that is in a qualitative agreement with the model proposed for the Si(7 7 10) staircase [4]. It can be assumed that defects on steps can play a substantial role in minimization of the number of the dangling bonds and energy of the triple step configuration defining the periodicity of the step array.

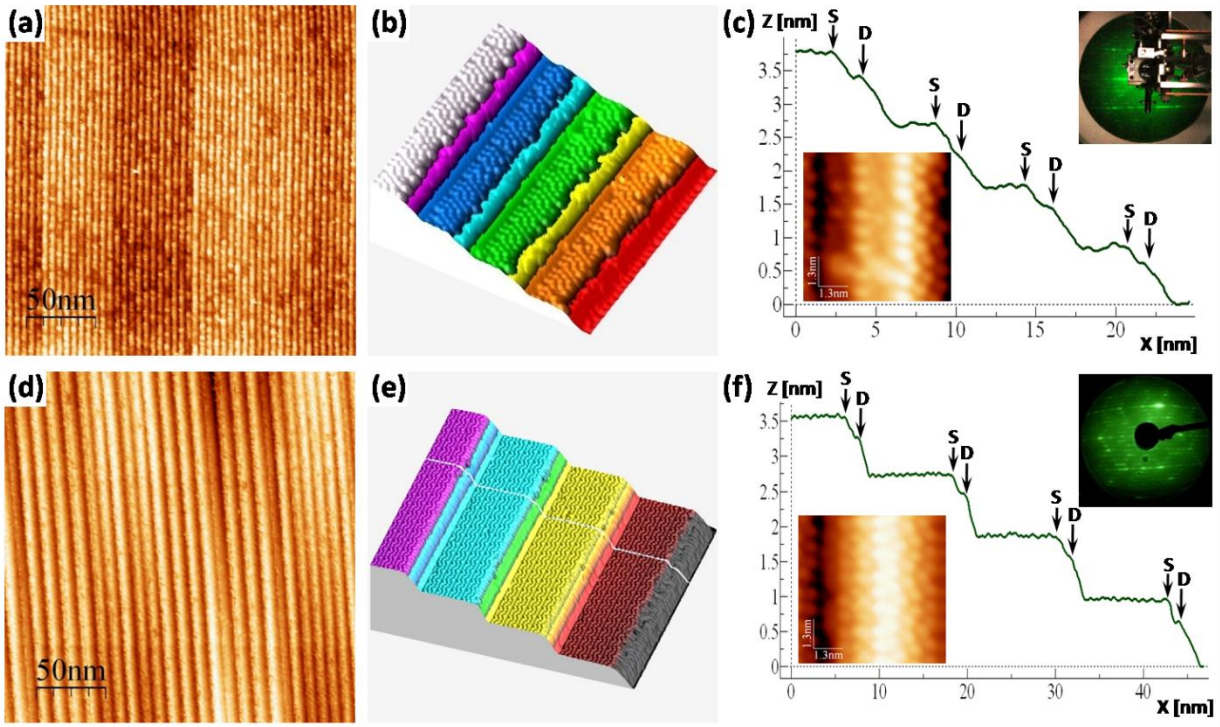

Fig.3. STM-images and atomic structure of the regular Si(557) (a-c) and Si(556) (d-e) triple step staircase. Cross-sections of the images (b) and (e), presented in (c) and (f), respectively, show the formation of single and double steps on Si(557) and Si(556) surfaces. Insets in (c) and (f) demonstrate LEED and STM images of triple steps for Si(557) and Si(556).

Fabrication of low-dimensional structures on vicinal Si(hhm) surfaces.

Si(hhm) surfaces containing regular systems of steps and terraces (Fig. 3) can be utilized for fabrication of 1D- and

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2D-structures of metal atoms with unique physical properties. The natural defects of the vicinal surfaces can be used for growth and experimental studies of atomic chains, systems of metallic wires with typical dimensions and periodicities in the nanometer scale, and anisotropic nanoscale islands on terraces of the semiconducting substrate. At submonolayer metallic coverages interaction of the deposited atoms with one another and with the substrate can lead to growth of either 2D islands or 1D atomic chains in certain crystallographic directions. The latter was observed for various metals on vicinal Si(111) surfaces [10-14, 22-28]. As an example, the feasibility of 1D atomic chain growth was demonstrated for gold [10-13], silver [14] and lead atoms [28] on Si(557) at submonolayer (Θ~0.2 ML) coverages. Using this vicinal silicon surface with large miscut off the Si(111) plane allowed to grow single domain atomic chain systems with one preferential chain direction along the step edges. Transport measurements conducted on these low dimensional structures [11-13] demonstrated a clear anisotropy of the conductivity parallel and perpendicular to steps at submonolayer metal coverages.

Figure 4 demonstrates anisotropic quasi-2D silver nanoislands grown on the terraces of the regular Si(557) triple step staircase [Fig. 3(a-c)] at monolayer coverages. As Figs. 4(a) and 4(b) illustrate, at small coverages (0-2 ML) islands grow on Si (111) terraces and have anisotropic shape with elongation along the step direction. The islands are spatially confined by the terrace width which is equal to three (inset on Fig. 3(c)) or four adatom rows (Fig. 3(f)) of the Si(111) 7×7 reconstruction depending on the exact triple step atomic structure. With increasing silver coverage [Fig. 4(b,c)] islands are mostly elongated along the step direction and confined in another direction by the Si(111) terrace width. However, some of the islands cover two or three neighbouring terraces [Fig. 4(c,d)]. At three different silver coverages deposited onto Si(557) surface [Fig. 3(a-c)] there is a preferential silver island height equal to 2 ML, as the histogram on Fig. 4(e) illustrates.

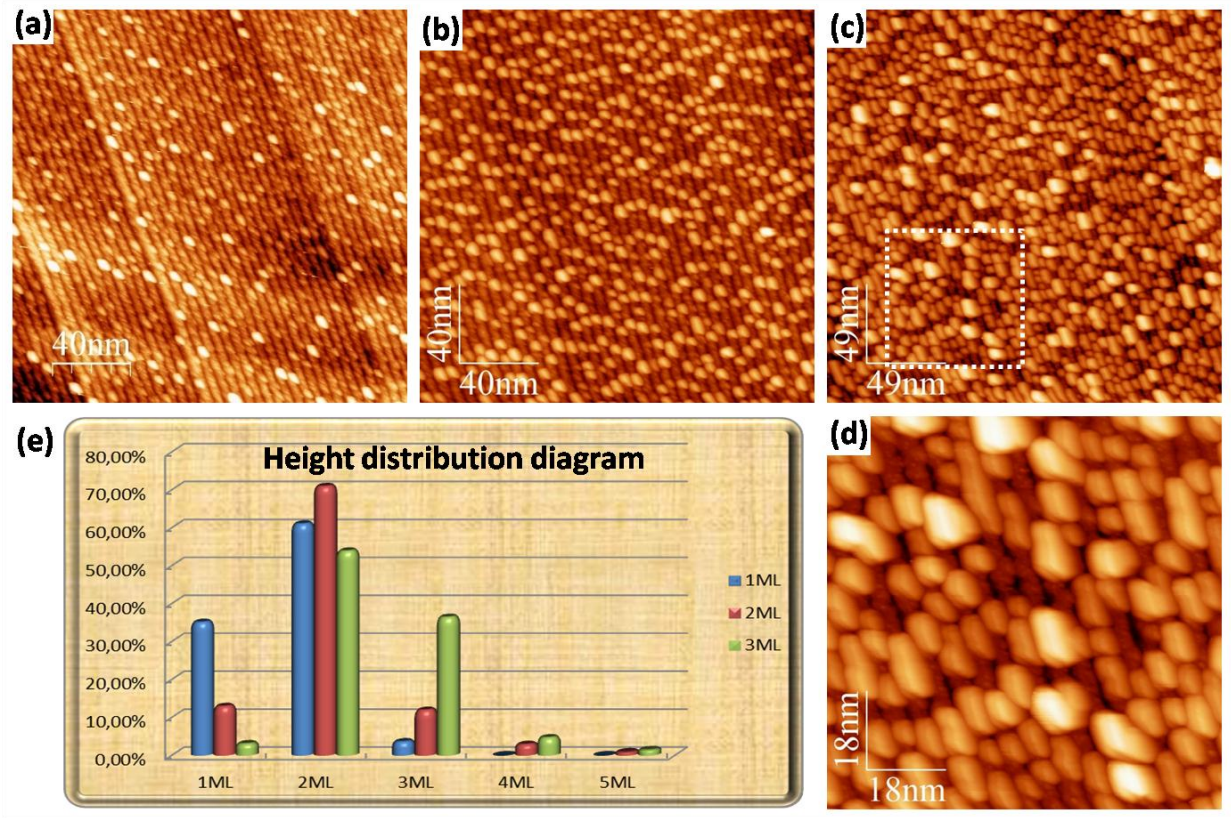

Fig. 4. (a-d) STM images of Ag/Si(557) at silver coverages of 1 ML (a), 2 ML (b) and 3 ML (c,d). (e) Histogram of Ag islands height distribution on Si(557) calculated from STM images measured at three different silver coverages.

Figure 5 demonstrates fabrication of quasi-1D atomic chain structures of gadolinium atoms using Si(hhm) stepped surfaces. As Figs. 5(a) and 5(b) illustrate, after a series of gadolinium depositions (0.1—0.2 ML) and annealings at 600ºC in the UHV chamber a regular array of quasi-1D Si(111)5×2-Gd structure with one preferential atomic chain

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direction can be fabricated on the Si(557) surface. Because of partial gadolinium diffusion into the bulk of silicon crystal, steps on Si(hhm) surfaces after deposition and annealing do not demonstrate perfect regularity as it was observed for clean Si(557) (Fig. 3) and Ag/Si(557) system (Fig. 4). Nevertheless, STM and LEED data [Fig. 5(a)] prove that chain-like atomic structures are elongated along the steps. In previous studies [25-27] fabrication of single- and three-domain (n×1) and (n×2) Yb/Si(111) [25], Eu/Si(111) [26] and Ce/Si(111) systems [27] has been demonstrated. However, controllable and reproducible growth of well-ordered single-domain structures of rare earth metals on silicon surfaces can be achieved using vicinal substrates distinguishing one of the <110> crystallographic directions.

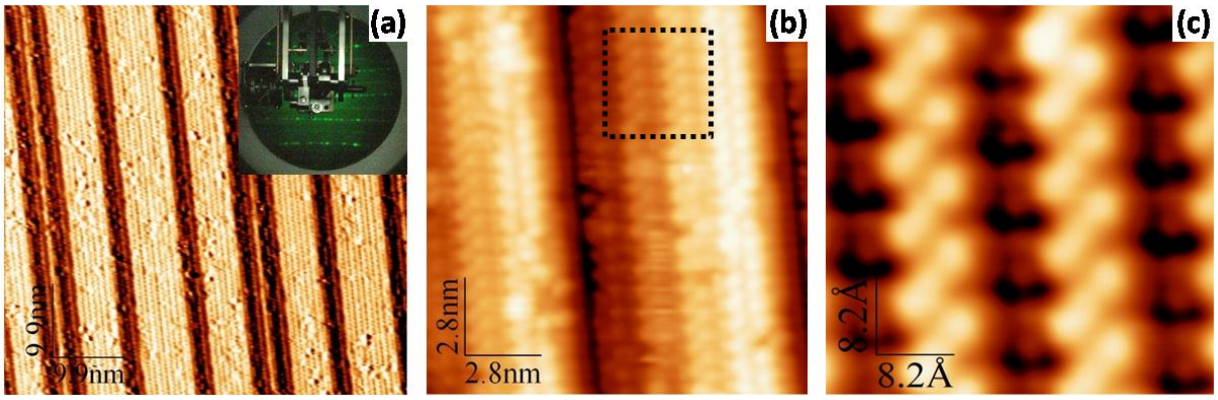

Fig. 5. (a-c) STM images of Si(557)+Gd 0.2 ML with one-dimensional 5×2 reconstruction on terraces. Image (a) is presented after differentiation to enhance the atomic contrast. Inset (a) – LEED picture of the Gd/Si(557)5×2. The area indicated by black square in (b) corresponds to panel (c).

4. CONCLUSIONS

We have demonstrated that application of special UHV annealing strategies allows to fabricate extremely regular triple step arrays with periods in the nanometer region on clean Si(hhm)7×7 surfaces. The results of our STM studies demonstrate the feasibility of fabrication of regular on atomic scale stepped templates without periodicity breaking on the surface area with lateral dimensions of several hundreds of nanometers. Atomically resolved STM data suggest the presence of several triple step configurations on Si(hhm) surfaces. Different step atomic structures were observed in STM experiments even on the surface regions containing regular Si(557) triple step array without periodicity breaking. Fabrication of low-dimensional (1D and 2D) structures of silver and gadolinium atoms on the vicinal Si(hhm) surfaces has been demonstrated.

5. ACKNOWLEDGEMENTS

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